

**MULTISTAGE DIFFERENTIAL AMPLIFIER WITH COMMONLY CONTROLLED INPUT AND OUTPUT COMMON MODE VOLTAGES**BACKGROUND OF THE INVENTION1. Field of the Invention

[0001] The present invention relates to differential amplifiers, and in particular, to differential amplifiers with a controllable common mode voltage.

2. Description of the Related Art

[0002] Signal amplifiers are used in many applications and may include amplifiers used for buffering or otherwise amplifying AC signals, as well as buffering or otherwise amplifying DC signals. One particular example of amplifiers used for DC signals includes those amplifiers used for generating reference voltages. Such reference voltage amplifiers are sometimes required to drive large circuit capacitances, such as those found in many analog signal systems. With such highly capacitive loads, it is difficult to achieve high DC gain and high bandwidth in an efficient manner. One common technique to address this problem is to use a differential amplifier. However, differential amplifiers require that both the input and output common mode voltages be controlled.

[0003] One widely used common mode control involves the placement of a voltage divider at the output of the amplifier. However, this reduces the DC gain of the amplifier, thereby requiring the use of a multistage amplifier to compensate for such gain reduction.

[0004] Another technique is the use of a multistage, or cascaded, transconductance ( $gm/gm$ ) amplifier. However, a cascaded transconductance amplifier will still have low DC gain and poor phase margin since the amplifier must be internally compensated. In an effort

to maintain DC gain by avoiding the use of a resistive output voltage divider, one technique involves a simple gate-averaging amplifier at the output to sense the output voltage and then apply a feedback voltage to correct the output common mode voltage. However, only the output amplifier stage benefits from this, leaving the auxiliary, or preceding, amplifier stage(s) with no common mode voltage control. As a result, the common mode voltage loop will have low DC gain and low bandwidth.

#### SUMMARY OF THE INVENTION

[0005] In accordance with the presently claimed invention, a multistage differential amplifier is provided with commonly controlled input and output common mode voltages. A shared common mode control signal jointly controls both input and output common mode voltages with a DC gain and bandwidth substantially equivalent to the differential signal gain and bandwidth.

[0006] In accordance with one embodiment of the presently claimed invention, a multistage differential amplifier with commonly controlled input and output common mode voltages includes differential input terminals, differential output terminals, a common mode control terminal, and differential amplifier circuits. First and second differential input terminals convey first and second phases of a differential input signal with an associated input common mode voltage. First and second differential output terminals convey first and second phases of a differential output signal corresponding to the differential input signal with an associated output common mode voltage. A common mode control terminal conveys a common mode control signal for jointly controlling the input and output common mode voltages. A plurality of differential amplifier circuits are successively coupled between the common mode control terminal, the first and second differential input terminals, and the first

and second differential output terminals. Each one of the plurality of differential amplifier circuits includes first and second amplifier input terminals, first and second amplifier output terminals, an input control terminal and an output control terminal. A first one of the plurality of differential amplifier circuits is coupled to the first and second differential input terminals via the first and second amplifier input terminals, and is further coupled to the common mode control terminal via the input control terminal. A last one of the plurality of differential amplifier circuits is coupled to the first and second differential output terminals via the first and second amplifier output terminals. The first and second amplifier input terminals and the input control terminal of each succeeding one of the plurality of differential amplifier circuits is coupled to the first and second amplifier output terminals and the output control terminal, respectively, of a preceding one of the plurality of differential amplifier circuits.

[0007] In accordance with another embodiment of the presently claimed invention, a multistage differential amplifier with commonly controlled input and output common mode voltages includes input differential amplifier circuitry, intermediate differential amplifier circuitry and output differential amplifier circuitry. The input differential amplifier circuitry includes: first and second input amplifier input terminals for reception of first and second phases of a differential input signal with an associated input common mode voltage; first and second input amplifier output terminals; an input amplifier control input terminal for reception of a common mode control signal; and an input amplifier control output terminal. The intermediate differential amplifier circuitry includes: first and second intermediate amplifier input terminals coupled to the first and second input amplifier output terminals; first and second intermediate amplifier output terminals; an intermediate amplifier control input terminal coupled to the input amplifier control output terminal; and an intermediate amplifier control output terminal. The output differential amplifier circuitry includes: first and second

output amplifier input terminals coupled to the first and second intermediate amplifier output terminals; first and second output amplifier output terminals for conveyance of first and second phases of a differential output signal corresponding to the differential input signal with an associated output common mode voltage corresponding to the input common mode voltage; an output amplifier control input terminal coupled to the intermediate amplifier control output terminal; and an output amplifier control output terminal.

[0008] In accordance with still another embodiment of the presently claimed invention, a multistage differential amplifier with commonly controlled input and output common mode voltages includes input amplifier means, intermediate amplifier means and output amplifier means. The input amplifier means is for receiving a common mode control signal and an input differential signal with an associated input common mode voltage and in response thereto providing a first intermediate differential signal and a first intermediate control signal, wherein the input common mode voltage is controlled by the common mode control signal. The intermediate amplifier means is for receiving the first intermediate differential signal and the first intermediate control signal and in response thereto providing a second intermediate differential signal and a second intermediate control signal. The output amplifier means is for receiving the second intermediate differential signal and the second intermediate control signal and in response thereto providing an output differential signal corresponding to the input differential signal with an associated output common mode voltage corresponding to the input common mode voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGS. 1A and 1B together are a schematic circuit diagram of a multistage differential amplifier with commonly controlled input and output common mode voltages in accordance with one embodiment of the presently claimed invention.

[00010] FIG. 2 is a signal diagram depicting the relationship between a common mode voltage and a differential signal.

[00011] FIG. 3 is a schematic circuit diagram of a transconductance amplifier for which the benefit of commonly controlled input and output common mode voltages can be realized.

DETAILED DESCRIPTION

[00012] The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

[00013] Throughout the present disclosure, absent a clear indication to the contrary from the context, it will be understood that individual circuit elements as described may be singular or plural in number. For example, the terms "circuit" and "circuitry" may include either a single component or a plurality of components, which are either active and/or passive and are connected or otherwise coupled together (e.g., as one or more integrated circuit chips)

to provide the described function. Additionally, the term "signal" may refer to one or more currents, one or more voltages, or a data signal. Within the drawings, like or related elements will have like or related alpha, numeric or alphanumeric designators.

[00014] Referring to FIGS. 1A and 1B together, a multistage differential amplifier with commonly controlled input and output common mode voltages in accordance with one embodiment of the presently claimed invention includes three amplifier stages S1, S2, S3 and two biasing stages B1, B2 biased between the power supply rails VDD, VSS. Input stage S1 and intermediate stage S2 are formed by three circuit branches having multiple telescopically coupled N-type metal oxide semiconductor field effect transistors (N-MOSFETs). Output stage S3 has three circuit branches made up of multiple complementary MOSFETs (C-MOSFETs). For example, transistor M272 in the first stage S1 is an N-MOSFET and transistor M300 in the output stage S3 is a P-MOSFET.

[00015] The input biasing stage B1 includes a current source IB1 which provides a current I1 to transistors M305 and M140. This causes a bias voltage VB1 to be generated at the gate terminals of transistors M140, M311, M307, M306, M284, M309, M308 and M289 of the input bias stage B1, input amplifier stage S1 and intermediate amplifier stage S2. Similarly, output biasing stage B2 includes a current source IB2 which provides a current I2 to transistors M299, M298 and M297. This causes a biasing voltage VB2 to be generated at the gate terminals of these transistors, as well as to the gate terminals of transistors M296, M293 and M89 of the output amplifier stage S3.

[00016] The input amplifier stage S1 receives the positive VIP and negative VIN signal phases of the differential input signal VI at the gate terminals of transistors M291 and M185. The common mode control voltage VCMO is applied to the gate terminal of transistor

M290 of the input amplifier stage S1, and to the gate terminals of transistors M305 and M312 of the input biasing stage B1.

[00017] In response to the application of the input differential signal phases VIP, VIN, the first amplifier stage S1 generates corresponding inverted signals /VIP and /VIN at the drain terminals of transistors M291 and M185, respectively. Similarly, application of the common mode voltage control signal VCMO causes a corresponding inverted control signal /VCMO to be generated at the drain terminal of transistor M290. These signals /VIP, /VIN, /VCMO drive the drain terminals of corresponding transistors in the second amplifier stage S2. This, in turn, results in further corresponding signals //VIP, //VIN, //VCMO to be generated at the drain terminals of transistors M304, M279 and M303. These signals //VIP, //VIN, //VCMO drive the gate terminals of corresponding transistors M46, M267 and M45 in the output amplifier stage S3, thereby generating the negative VON and positive VOP signal phases of the output signal VO, and a corresponding common mode control voltage //VCMO at the drain terminals of transistors M46, M267 and M45, respectively. As a result, it can be seen that the common mode control signal VCMO applied at the input amplifier stage S1 propagates through each amplifier stage S1, S2, S3 so as to control the common mode voltages for the input signal VI and the output signal VO, as well as for each of the intermediate, or interstage, signals /VI, //VI.

[00018] The input amplifier stage S1 also includes a shared terminal formed by the mutual connection of the source terminals of transistors M291, M290 and M185. Similarly, intermediate amplifier stage S2 has a shared terminal formed by the mutual connection of the source terminals of transistors M304, M303 and M279, as does the output amplifier stage S3 by the mutual connection of the source terminals of transistors M46, M45 and M267.

[00019] Further discussion of an amplifier similar to this can be found in US Patent No. 6,445,250, a disclosure of which is incorporated herein by reference.

[00020] With reference to FIG. 2, a multistage differential amplifier in accordance with the presently claimed invention allows the common mode voltage VCM of a signal to be controlled for both the input and output signals of the amplifier. In accordance with the presently claimed invention, a single common mode control voltage provides joint control at both the input and output terminals of the amplifier, thereby achieving DC gain and bandwidth substantially equivalent to the gain and bandwidth of the differential signal being amplified.

[00021] Referring to FIG. 3, one application, among others, for which the amplifier circuit of FIGS. 1A and 1B is well suited is that of a transconductance amplifier. Using the amplifier of FIGS. 1A and 1B as the operational amplifier (OP AMP), with feedback resistors R0 and R1 connected between the signal terminals for the input signal phases VIP, VIN and output terminals for the output signal phases VON, VOP, as shown, reference voltages V0, V1 can be generated across the output capacitors C0, C1 with the application of input currents I0, I1 at the input signal terminals. Ideally, the current sources I0, I1 should be well matched, as should the feedback resistors R0, R1, so as to ensure that the output common mode voltage is equal to the input common mode voltage.

[00022] Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods

within the scope of these claims and their equivalents be covered thereby.